Experiences Adapting Structures Codes
for Parallel & FPGA Speedup*

from **NASA Reconfigurable Scalable Computing**

to **Accelerating ORNL High Performance Computing**

by

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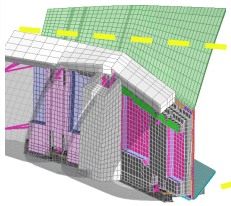
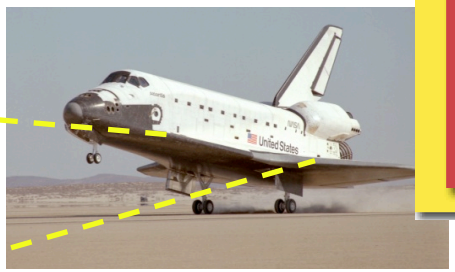
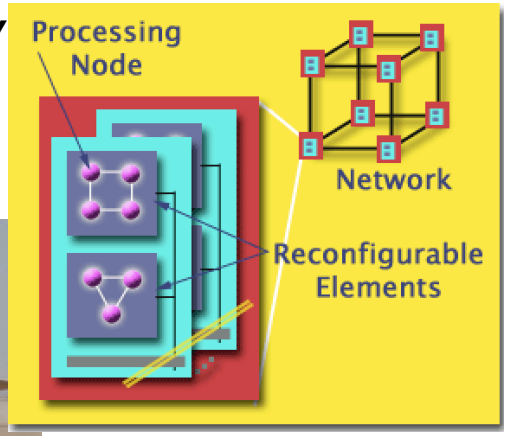
Oak Ridge National Laboratory, Tennessee

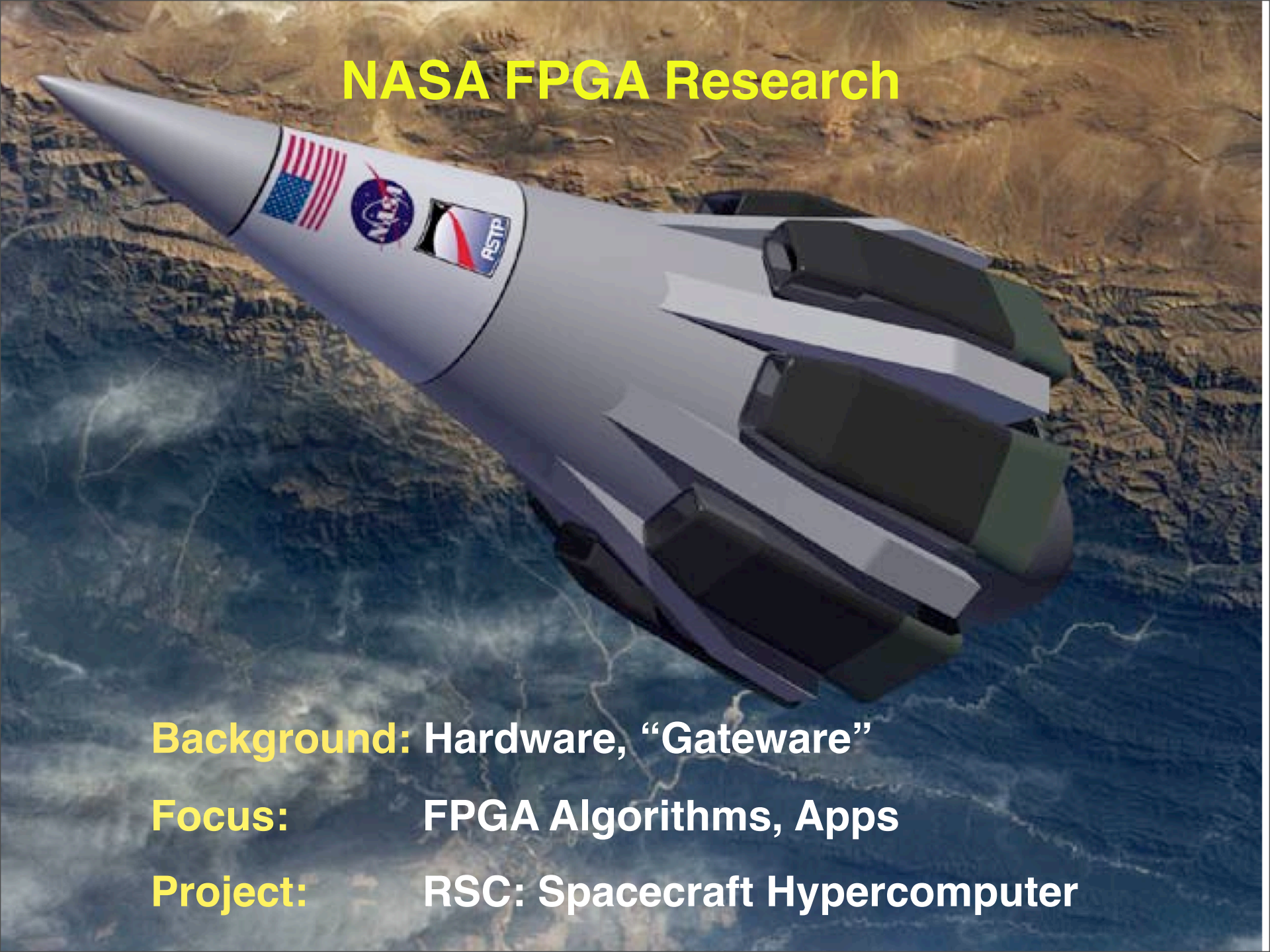
*Field-Programmable Gate Array







NASA FPGA Research

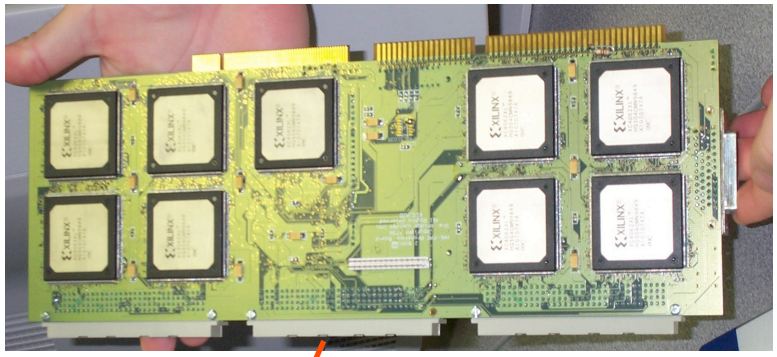


Background: Hardware, “Gateware”

Focus: FPGA Algorithms, Apps

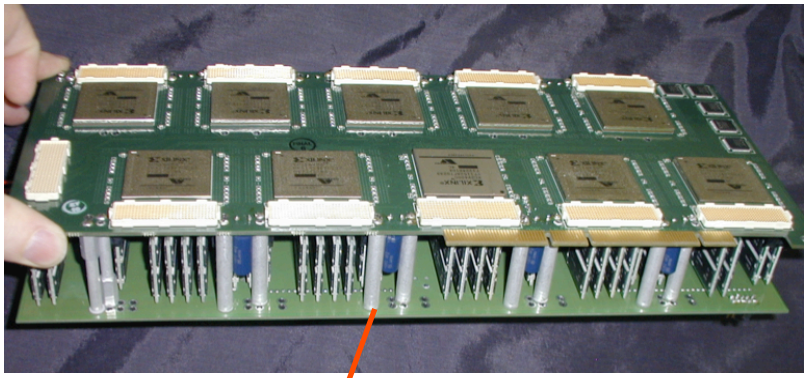
Project: RSC: Spacecraft Hypercomputer

NASA Reconfigurable Hypercomputers



62K gates/FPGA

'02



6M gates/FPGA

'04

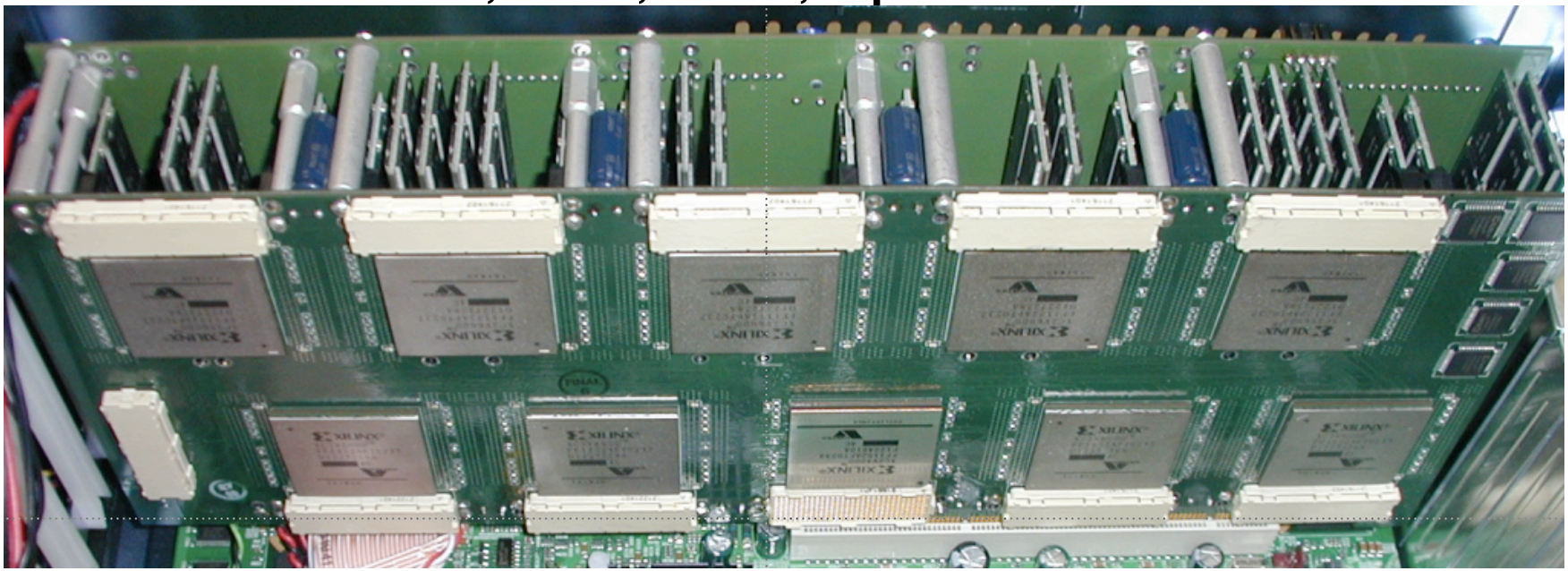
GOAL: Compute *Faster* *Without CPUs*

TEAM: Drs. Olaf Storaasli, Jarek Sobieski & Robert Singleterry,

Dave Rutishauser, Joe Rehder, Garry Qualls, Robert Lewis

Students: *MIT Harvard VT* Brown *UVA JPMorgan* Case Pitt, Governor's School

PARTNERS: Starbridge Systems (FPGA H/W + VIVA S/W)
NSA, USAF, MSFC, AlphaStar



Why FPGAs?

	Microprocessor (P4)	FPGA(2VP100)	
Clock Speed	3.8GHz	180MHz	-
Internal Memory Bandwidth	122 GBytes per Sec	7.5 TBytes per Sec	+
# Floating Point Units	2	146	+
Power Consumption	>100 WATTS	<10 WATTS	+
Peak Performance	7.6 GFLOPs	26 GFLOPS	+
Sustained Performance	0.76 GFLOPs	13 GFLOPS	+
I/O / External Memory Bandwidth	8.5 GBytes/sec	67 GBytes/sec	+

Courtesy: www.nallatech.com

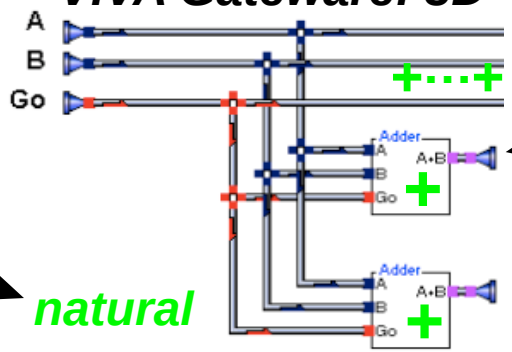
VIVA: *Custom Chip Design*

What: Graphically code FPGAs: *drag & drop* vs *text*)

Traditional Code: 1D

```
do i = 1, 1000
   C= A+B
end do
```

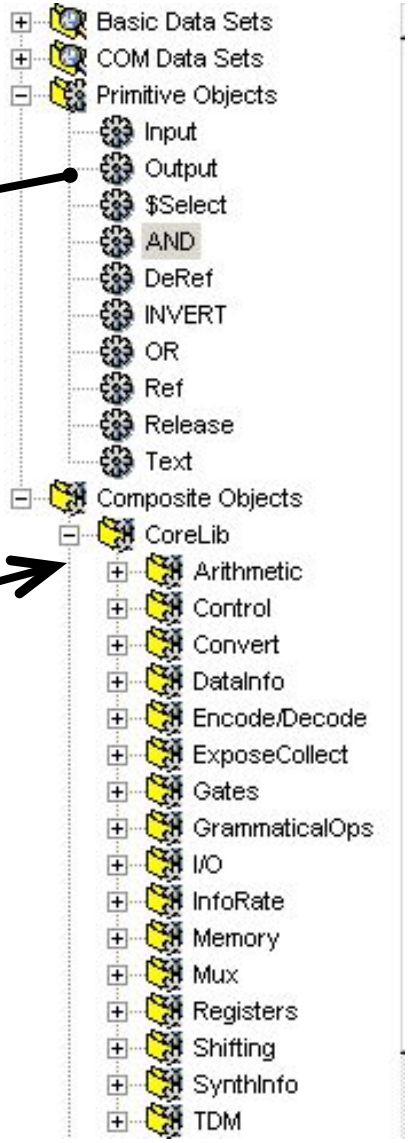
VIVA Gateware: 3D



Parallelism

esoteric ***natural***

VIVA Menu



How: Converts *icons-transports* to FPGA circuit

Why: near-ASIC speed (w/o chip design $$$)

Corelib: Pre-built objects & examples

Data: Any type-size-precision (not fixed)

System Description: ports to any hardware

"write once, run anywhere"

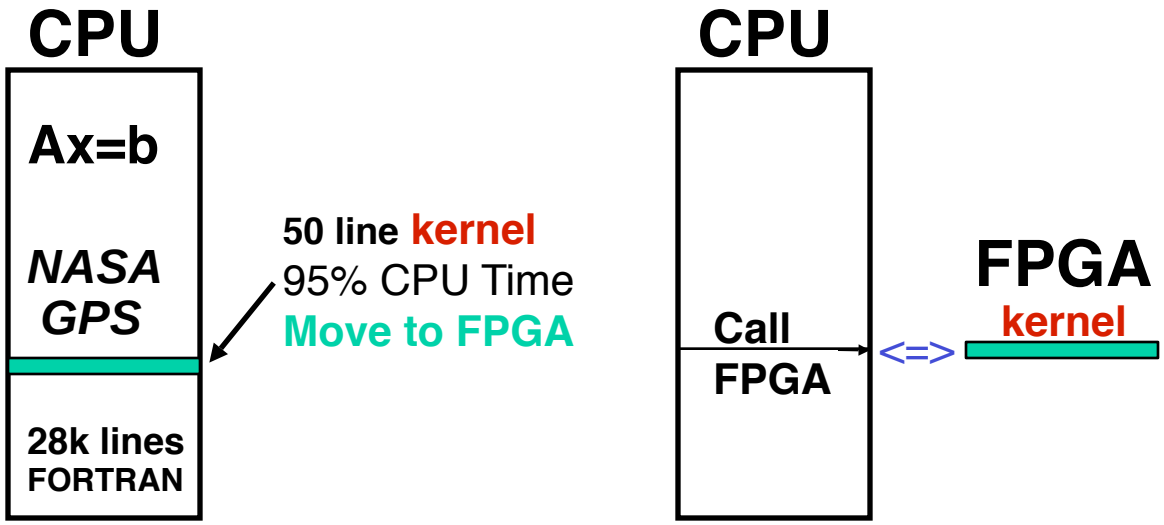
FPGA Options

CPU + FPGA Accelerator

Exploit kernel Parallelism Ops/cycle
C/FORTRAN calls VIVA kernel
Limit: FPGA gates + Amdahl's Law

Replace CPUs

Exploit Full Parallelism
Maximize Ops/cycle => Fill FPGA
VIVA/VHDL/Verilog code
Limit: FPGA(s) gates



GENOA-GPS* "Port"

GENOA *Analysis/Design (AlphaStar)*

Progressive Failure, Reliability, Durability
Manufacturing,Virtual Test, Life prediction

Calls GPS

Shuttle re-entry wing damage analysis time:
660 hours => minutes (Goal)

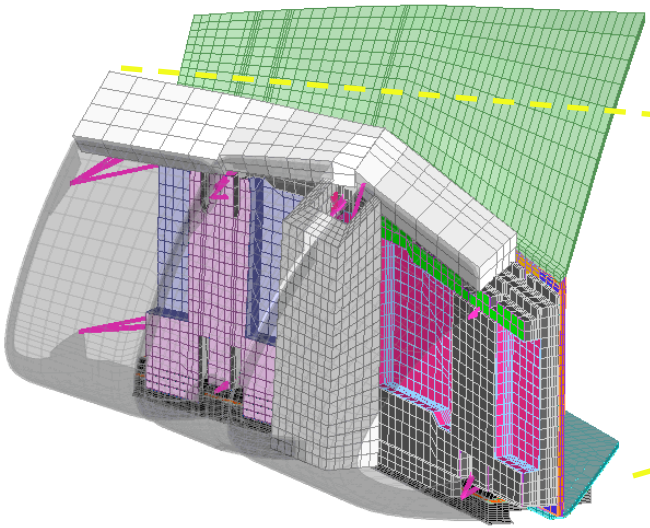
GPS *Matrix Equation Solver (NASA)*

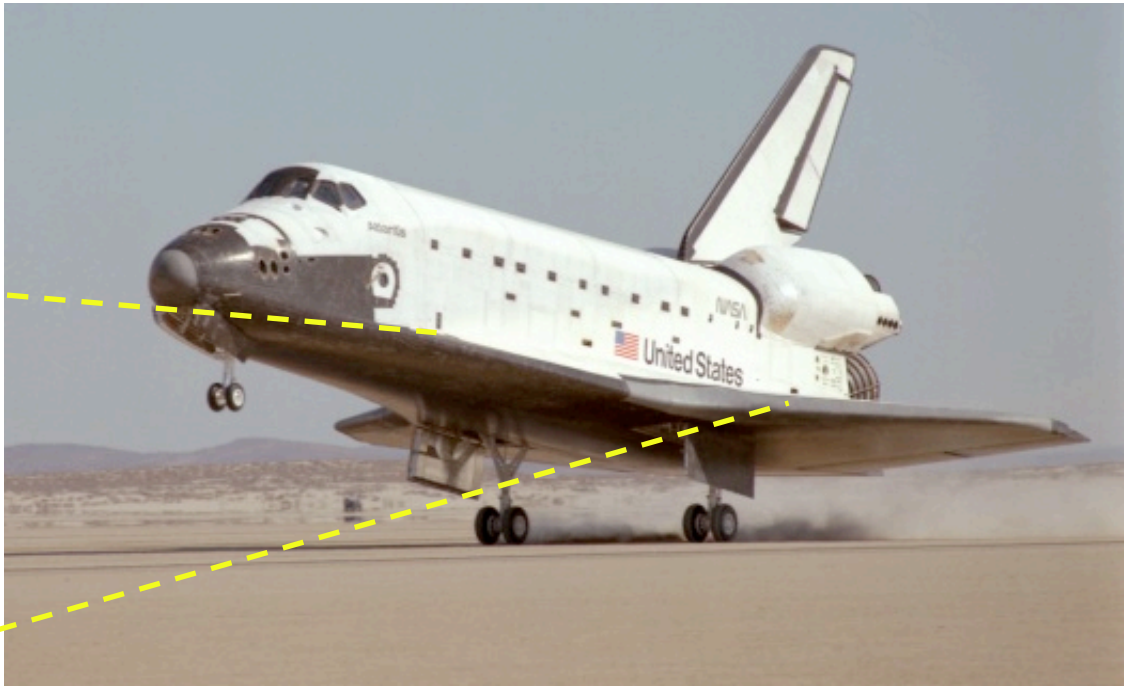
Structural, EM, acoustic analysis+design

Most Computations in 50-line kernel

kernel coded: VIVA-GPS
VIVA2.4 => large applications *ongoing*
(NASA-AlphaStar-Starbridge)

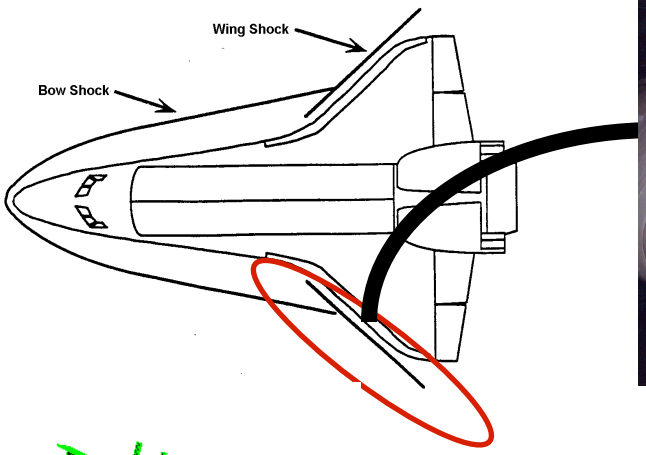
Finite Element Model

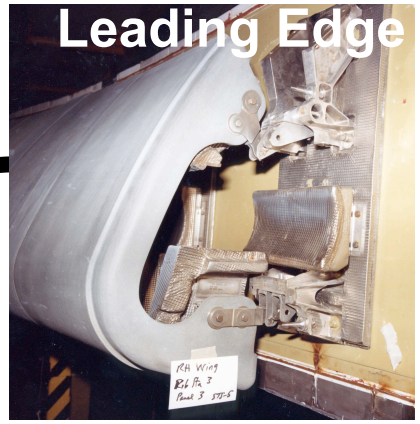




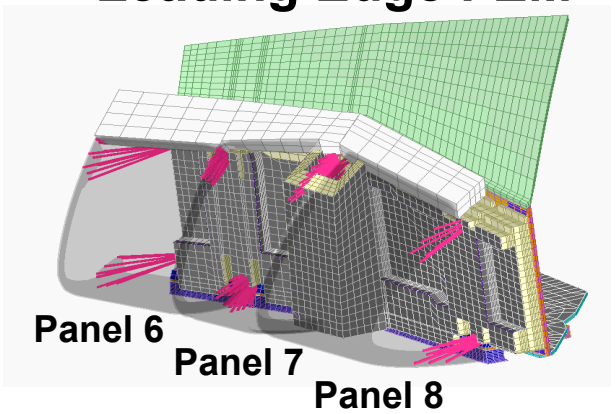
*'99 NASA Software-of-the-Year

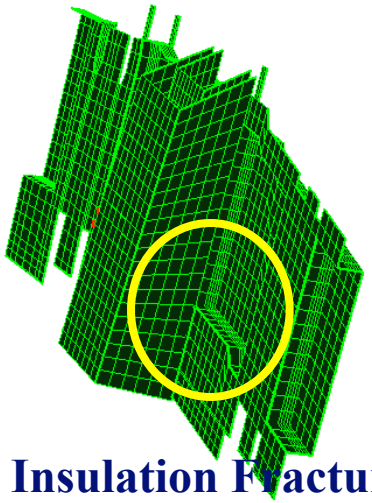
Columbia Burn-thru Analysis



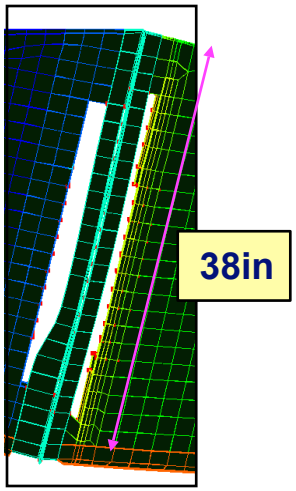


Leading Edge FEM

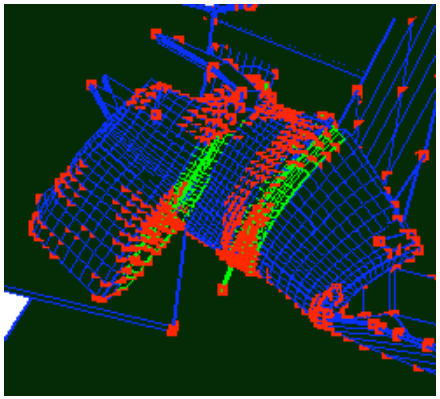




Insulation Fracture
230 Sec



Spar Fracture
500 sec



RCC-Tseal Fracture
503 sec

Time

FPGA Use

CPU +FPGA Accelerator

Exploit *Local* Parallelism
Max {kernel Ops/cycle}
C/FORTRAN calls VIVA kernel
Limit: FPGA gates + Amdahl's Law

Replace CPUs

Exploit Parallelism *Fully*
Max {Ops/cycle} => Fill FPGA
100% VIVA code
Limit: FPGA(s) gates

Maximize Performance via Parallelism

Adds/FPGA	16	32	128	256	512	640
% FPGA used	1	2	8	16	41	51
10^9 Ops	4	8	34	77	154	192

1000+ adds/clock cycle => 10^{11} Ops/sec

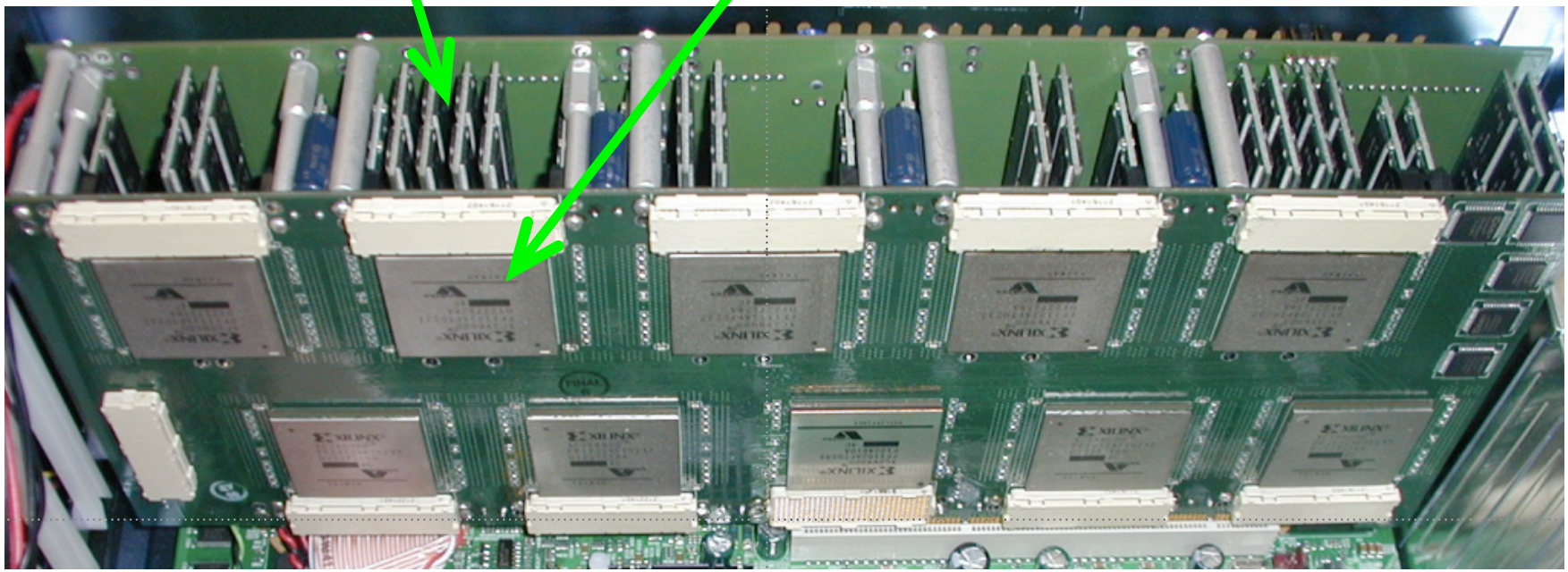
(1 add/cycle on CPUs)

Memory: FPGA & SDRAM

- keep "action" on/near FPGA -

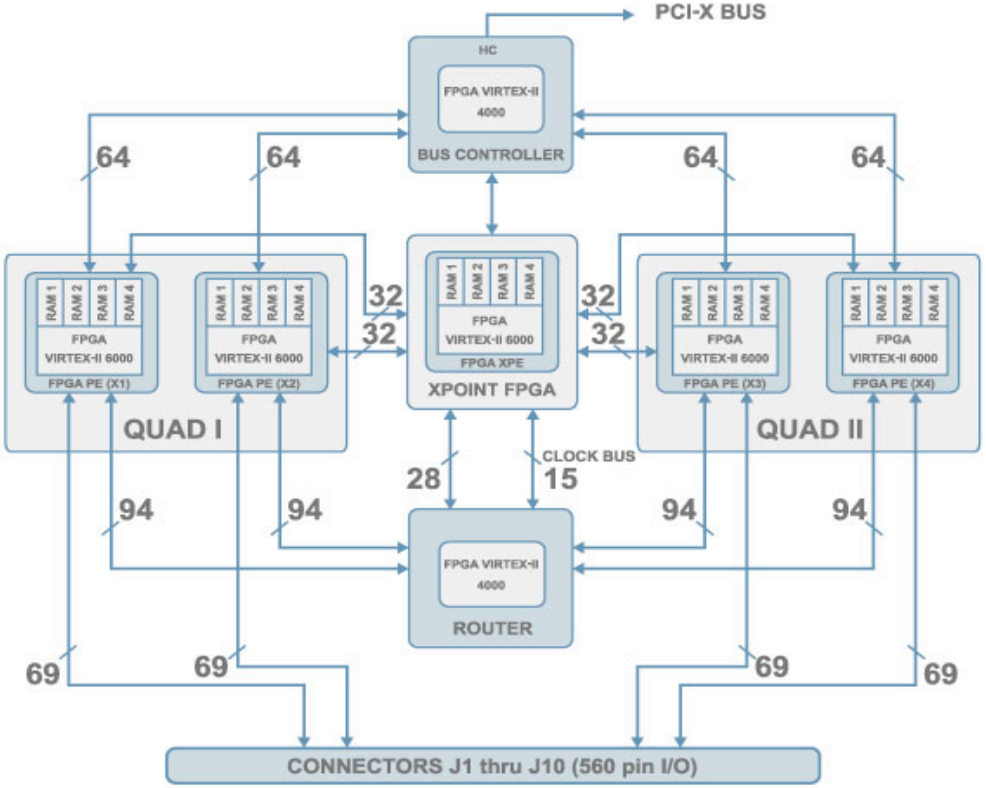
2-8GB SDRAM
(large applications)

144x 2KB blocks RAM



- User configures in VIVA for any data type (fixed, float …)

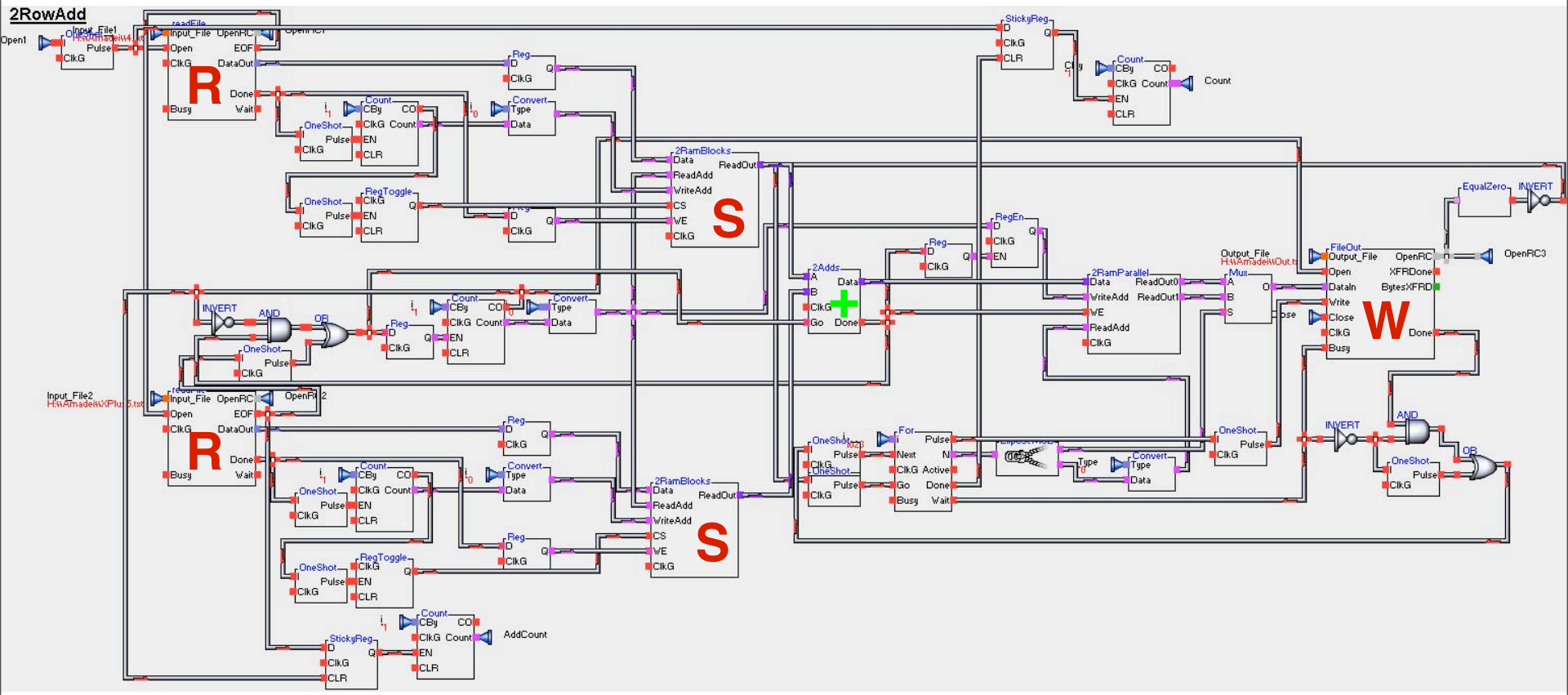
Langley's HC–36



- 4 user FPGAs on network (3 for I/O)
- Use Remote Desktop "Console" (PC, Mac, ...) on Net

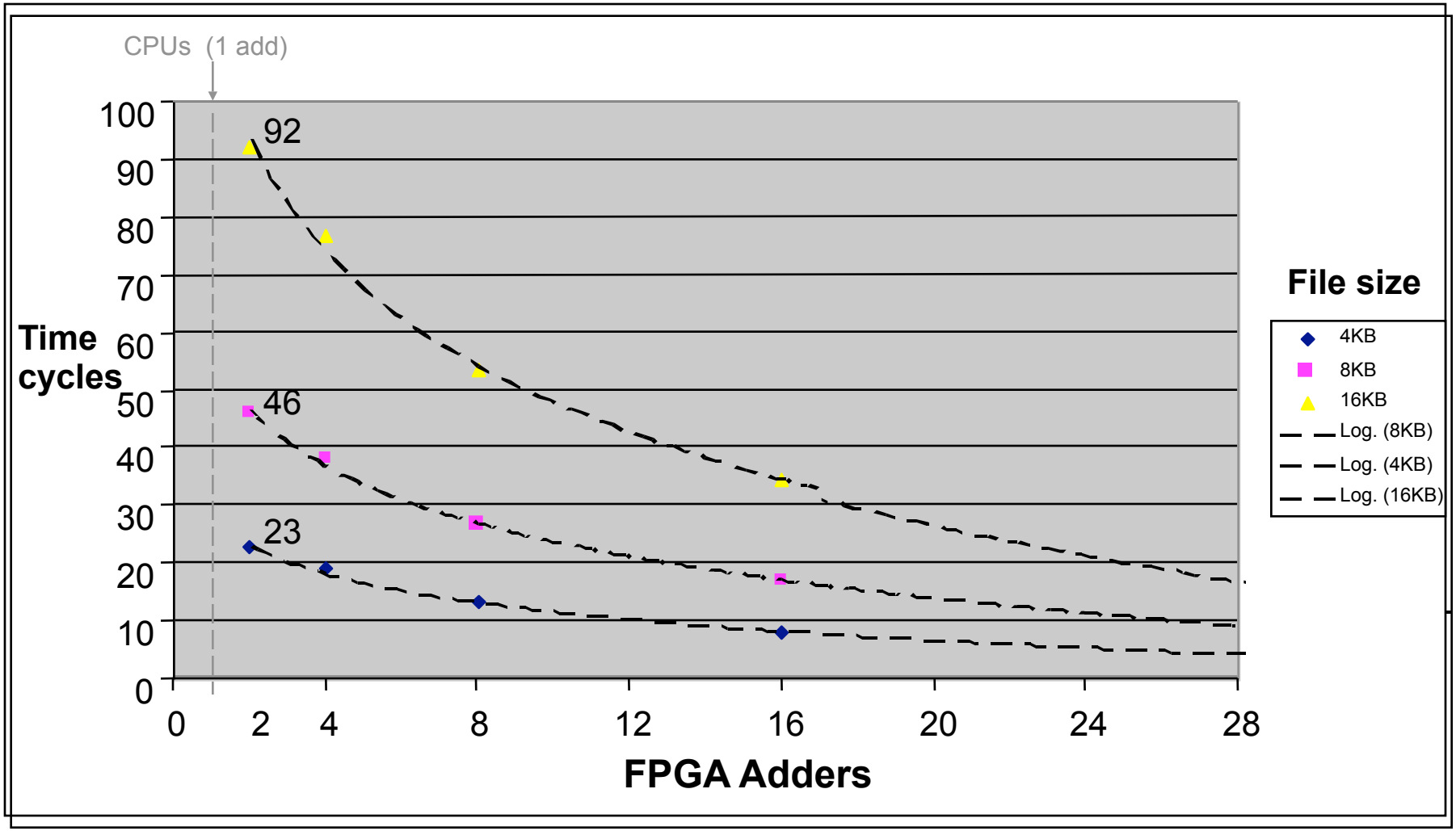
Add Files in Parallel

Read 2 files => Store in FPGA RAM => + files => Write result



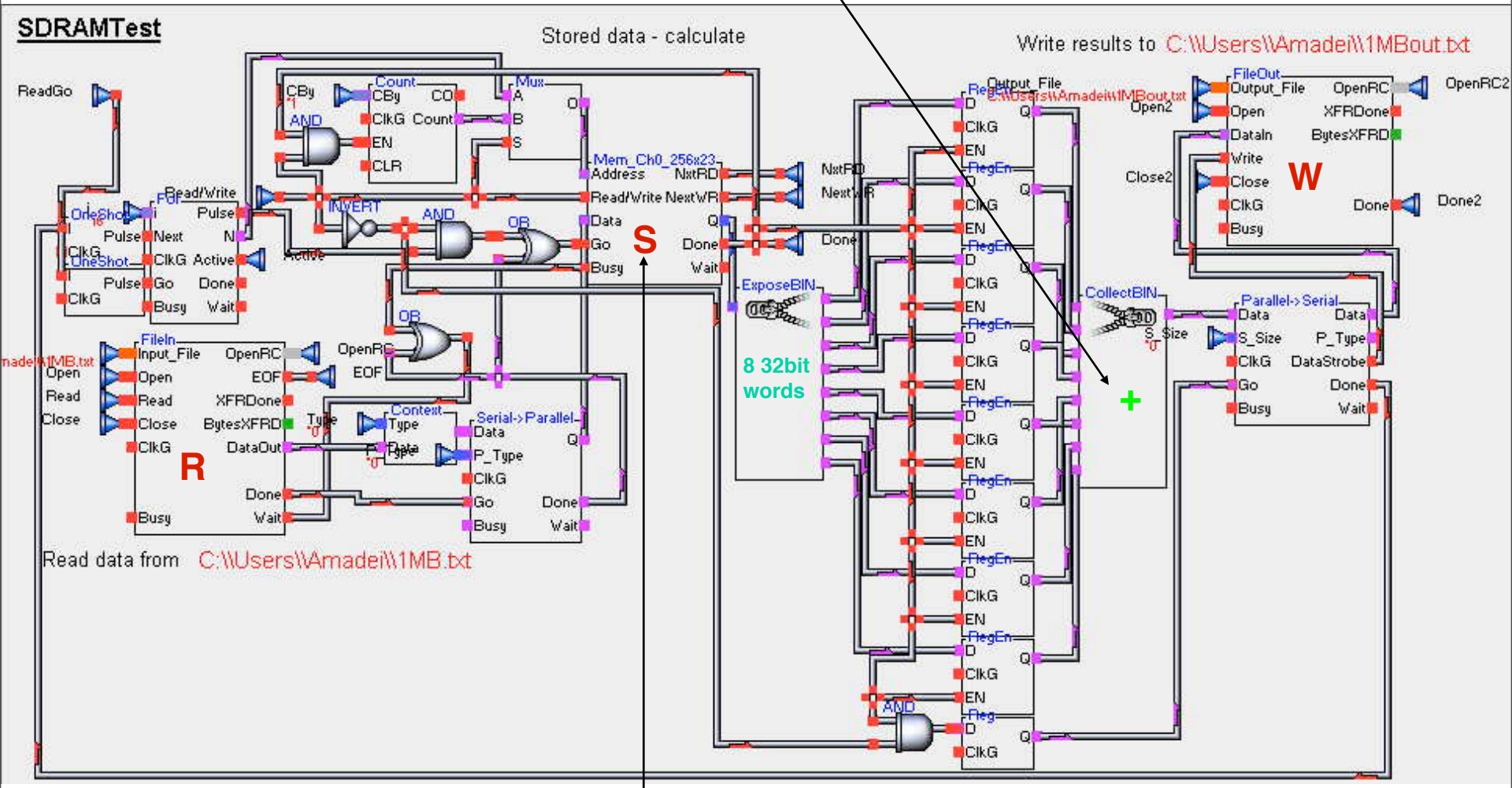
Parallel Adds Faster

- 4KB, 8KB 16KB files -



SDRAM Use

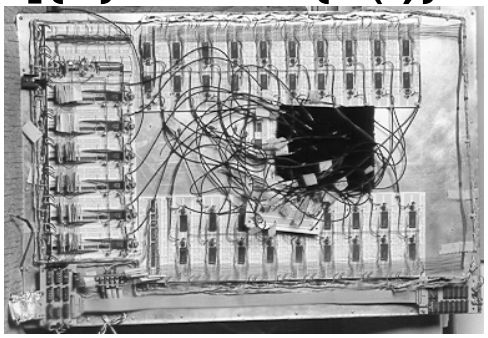
Read file => Store in SDRAM => (+ files =>) Write result



SDRAM: 256 (bits) x 2^{23}(memory locations) = 256MB/channel

Algorithms Developed

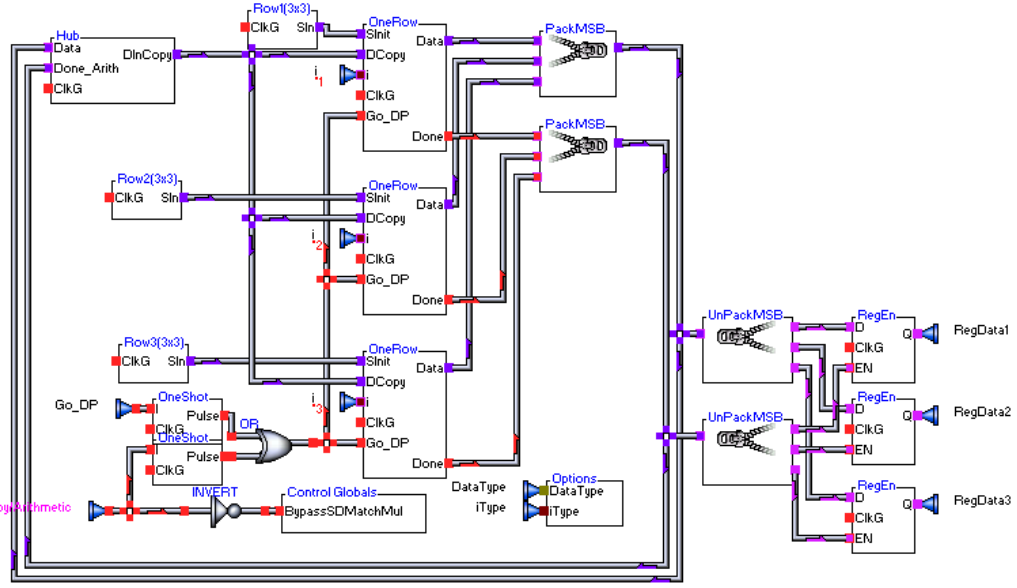
- **Matrix Algebra**: {V}, [M], $\{V\}^T\{V\}$, [M]x[M],GCD,…
  - **n!** => Probability: Combinations/Permutations
  - **Cordic** => Transcendentals: sin, log, exp, cosh…
- $\partial y/\partial x$ & $\int f(x)dx$ => Runge-Kutta: CFD, Newmark Beta: CSM
- **Matrix Equation Solvers**: [A]{x} = {b}, Gauss & Jacobi
  - **Dynamic Analysis**: $[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} + NL = \{P(t)\}$
  - **Analog Computing**: digital accuracy
  - **Nonlinear Analysis**: reduces NL time



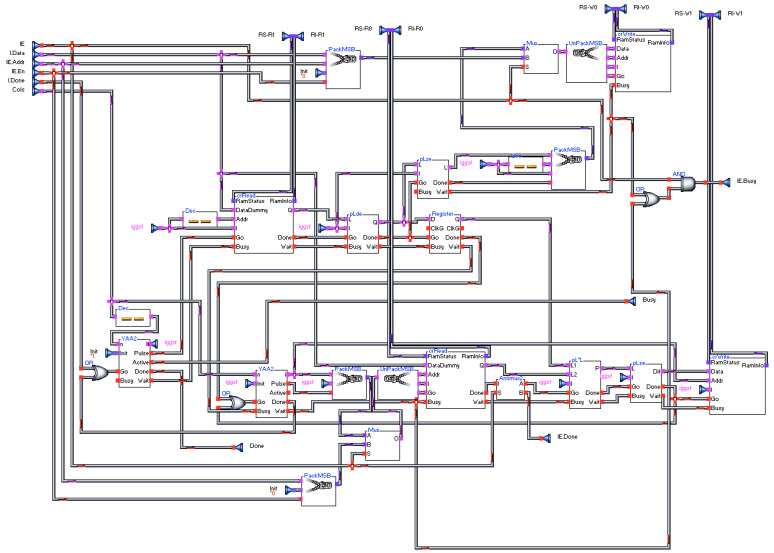
- **Structural Design & Optimization**

Applications: VIVA Code

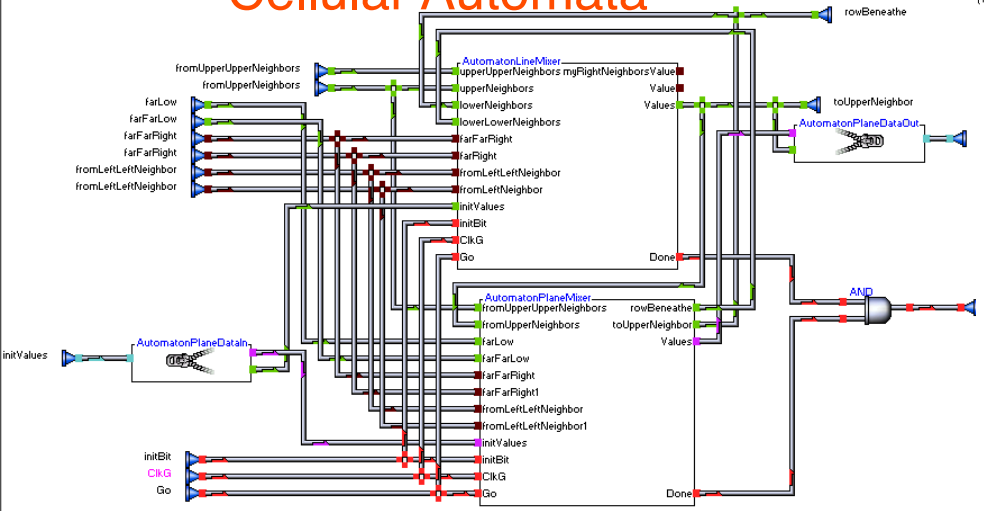
Jacobi Matrix Solver



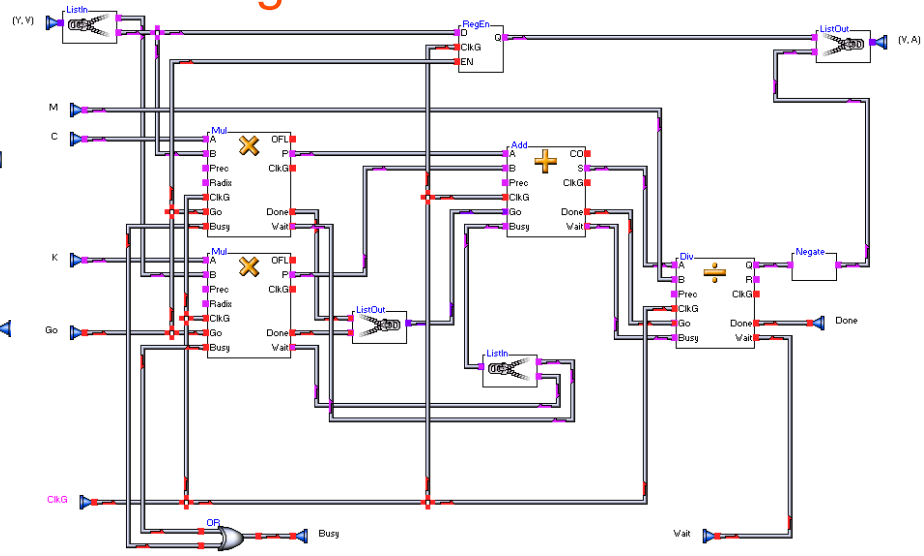
Gauss Matrix Solver



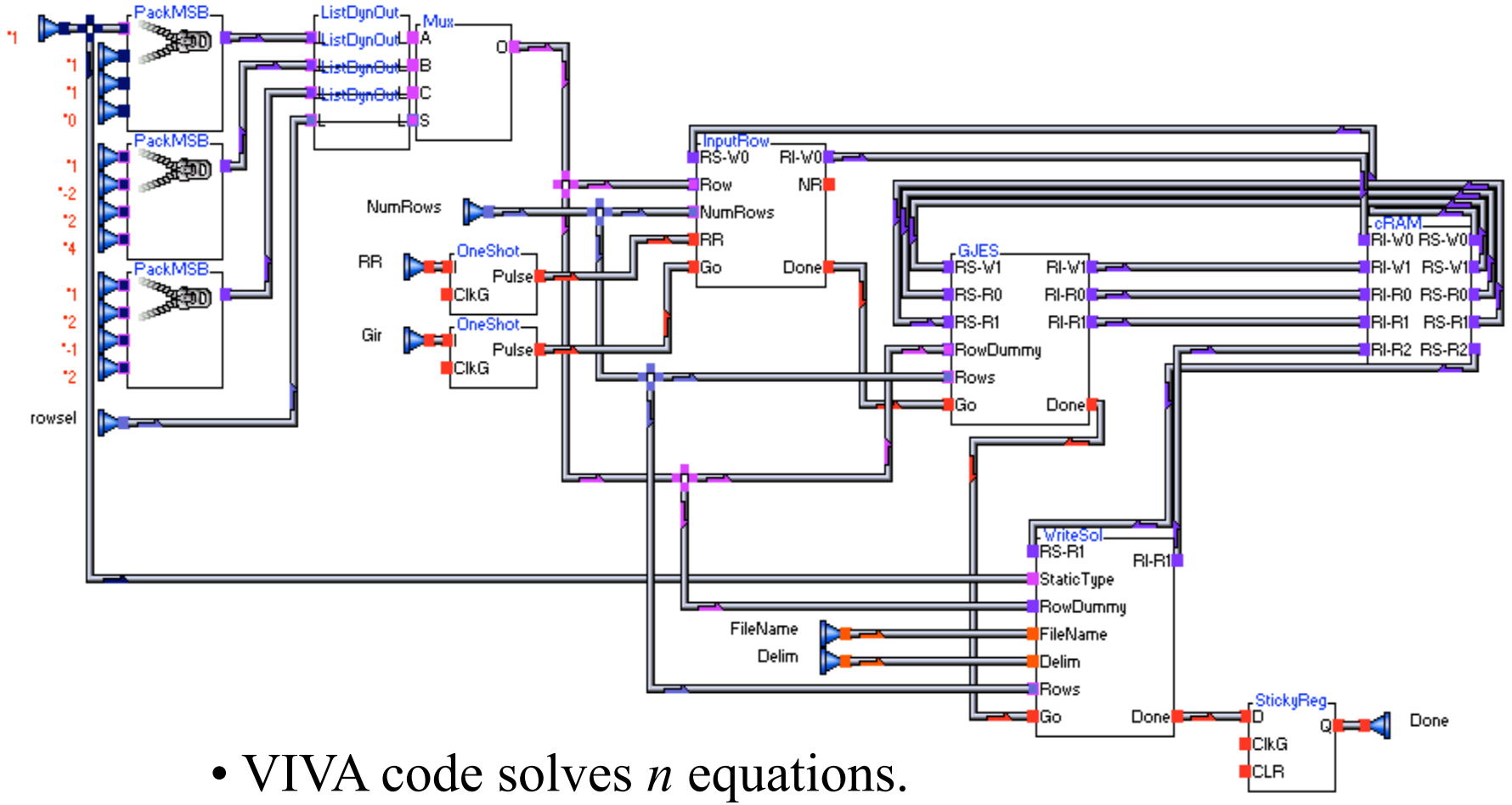
Cellular Automata



Runge-Kutta



Gauss-Jordan $\mathbf{A}x = \mathbf{B}$ Solver

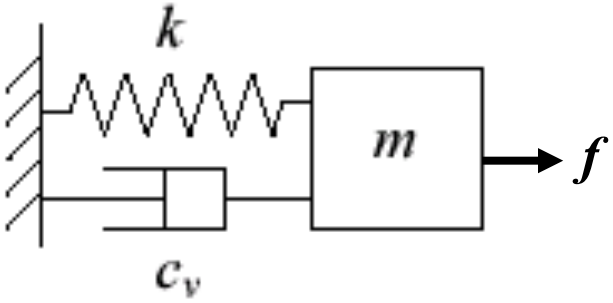


- VIVA code solves *n* equations.

Ex:
$$\begin{aligned} x_0 + x_1 + x_2 &= 0 \\ x_0 - 2x_1 + 2x_2 &= 4 \\ x_0 + 2x_1 - x_2 &= 2 \end{aligned} \quad \Longrightarrow \quad \begin{aligned} x_0 &= 4 \\ x_1 &= -2 \\ x_2 &= -2 \end{aligned}$$

- Run 1st on PC (emulator), then FPGA

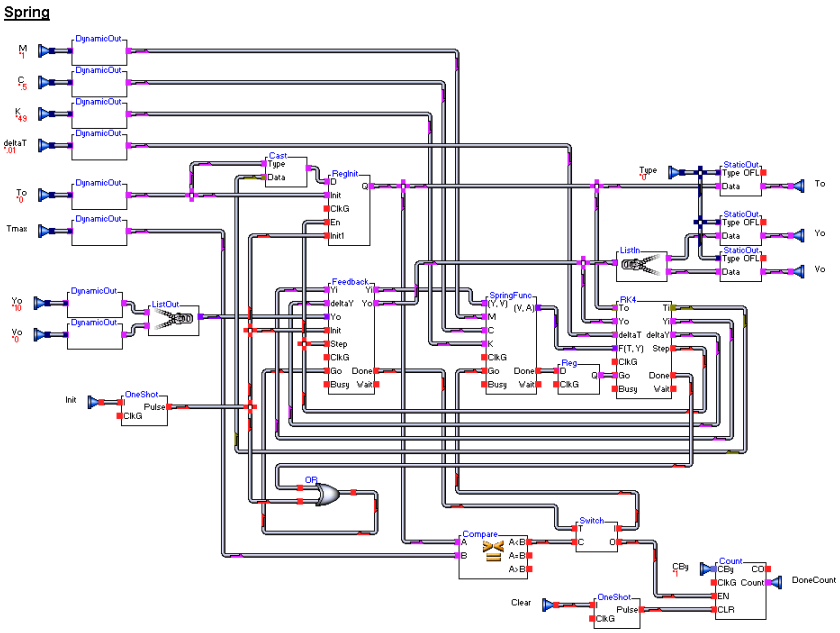
Spring-Mass Solver

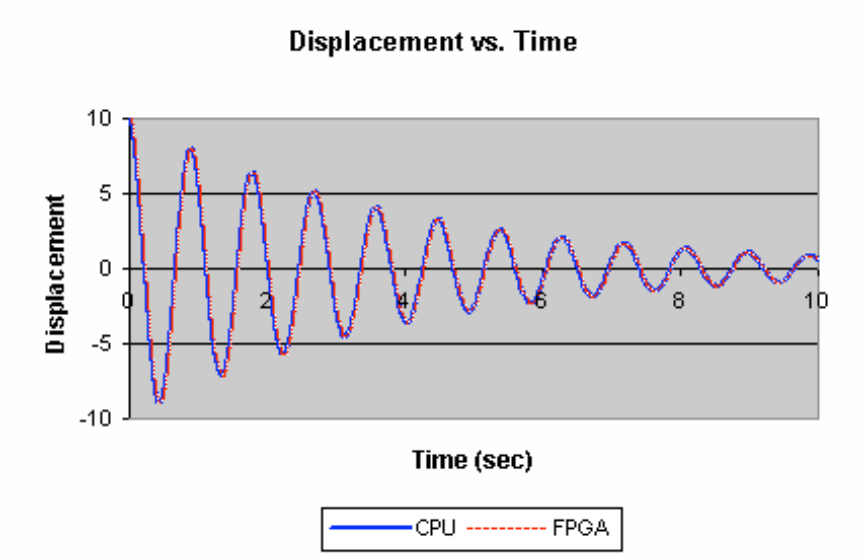


Method: 4-stage Runge-Kutta

$$\frac{du}{dt} = f(u,t) \qquad y(x_0) = y_0$$

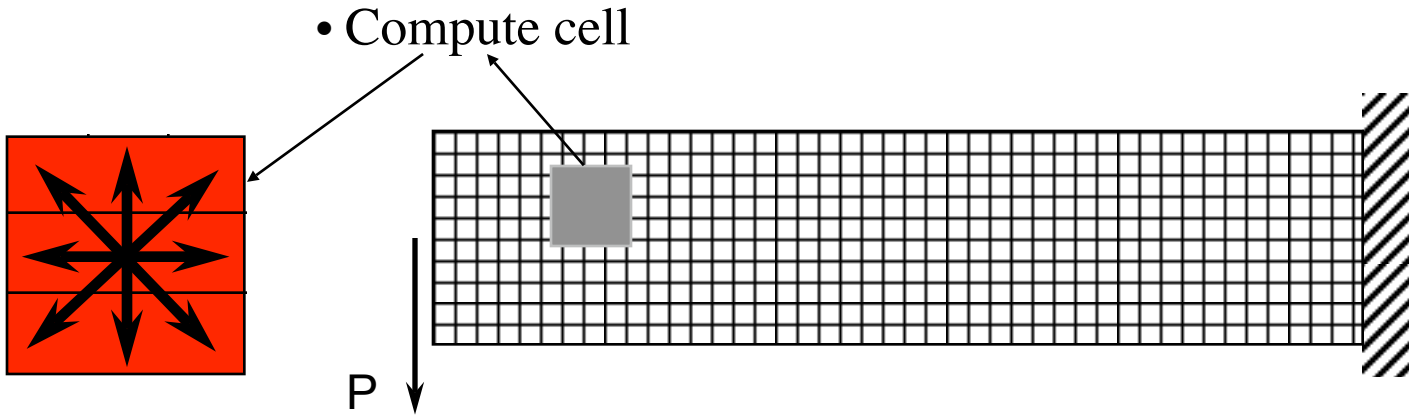
$$k_1 = hf(x_n, y_n)$$
$$k_2 = hf(x_n + \tfrac{1}{2}h, y_n + \tfrac{1}{2}k_1)$$
$$k_3 = hf(x_n + \tfrac{1}{2}h, y_n + \tfrac{1}{2}k_2)$$
$$k_4 = hf(x_n + h, y_n + k_3)$$
$$x_{n+1} = x_n + h$$
$$y_{n+1} = y_n + \tfrac{1}{6}(k_1 + 2k_2 + 2k_3 + k_4)$$



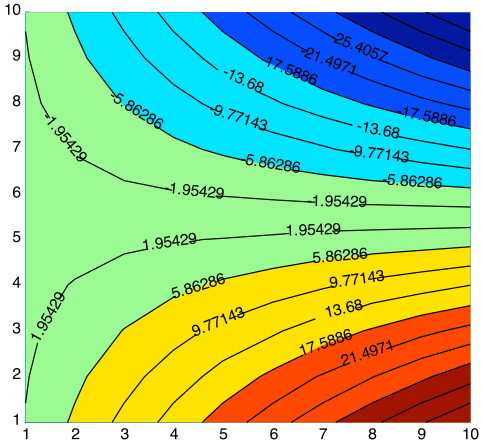


Cellular Automata

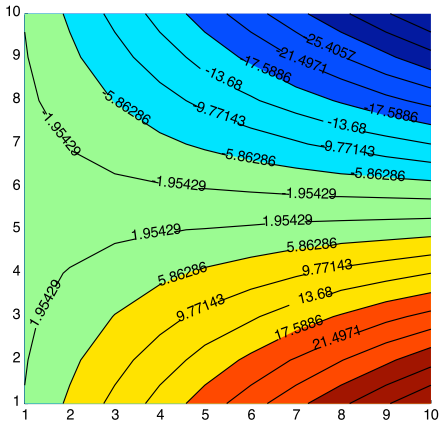
- Stephen Wolfram - *A New Kind of Science* => **Inherently Parallel**
- Complexity via **cell interactions** **w/o PDEs**
- CFD => Structures



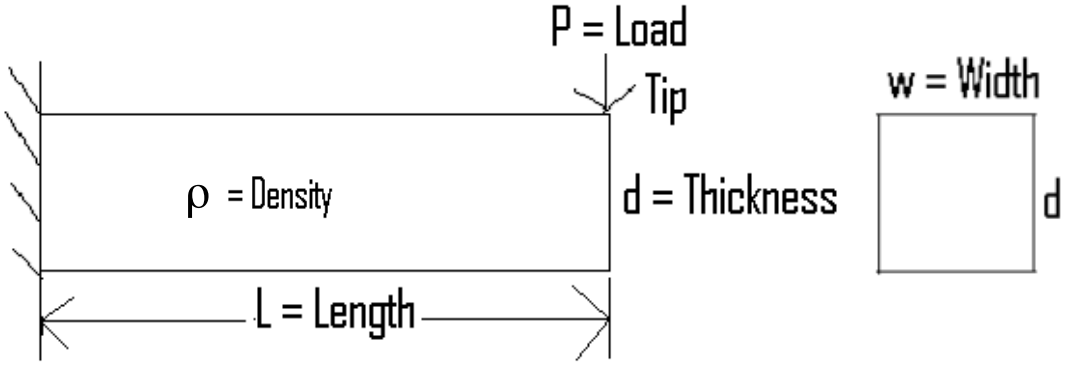
FEA solution



Cellular Automata solution



Cantilever Beam Optimization



Constants:

L = 24” W = 3” P = 20 lbs

ρ = 0.097 lbs/in^3

Constraint:

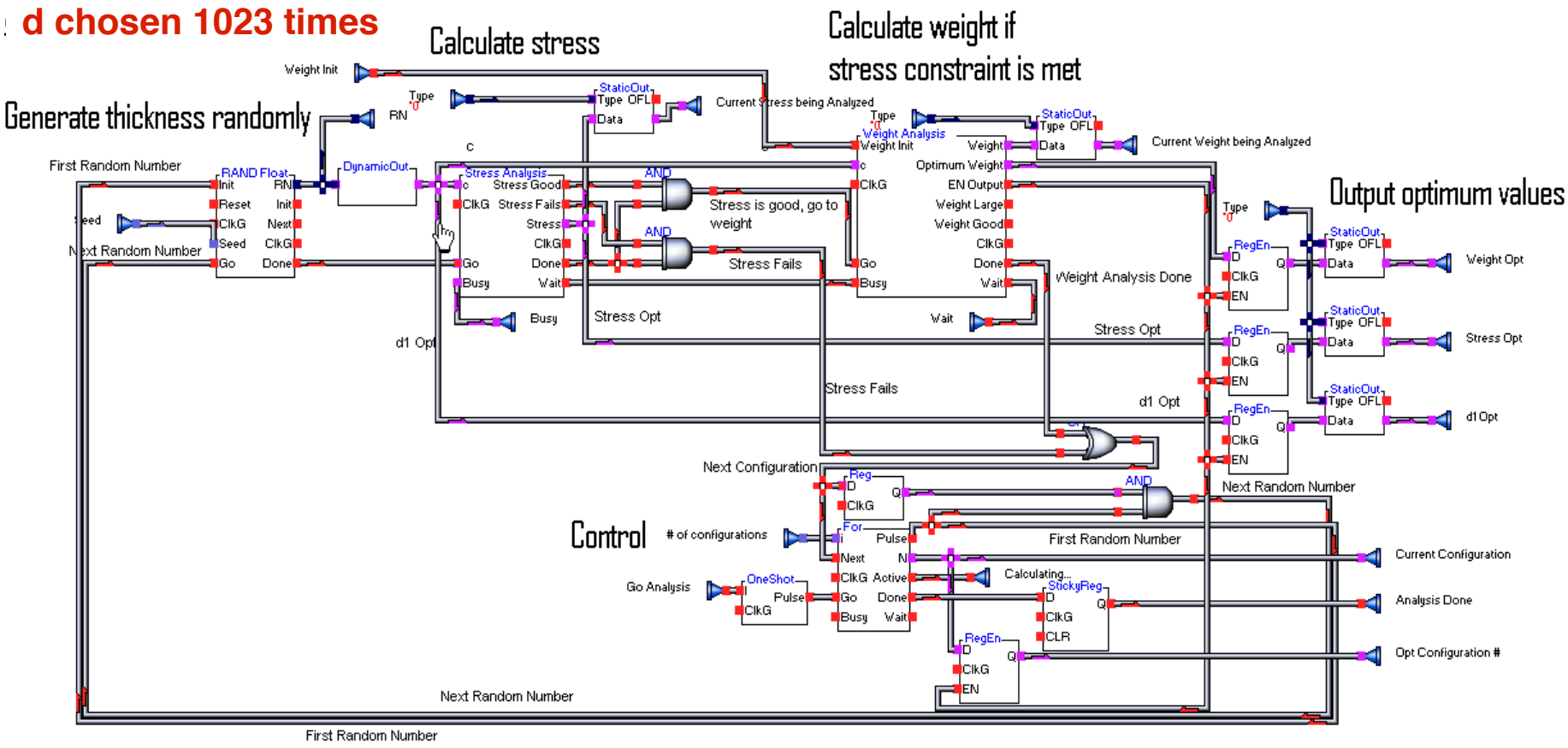
$Stress_{allowed}$ = 40K lbs/in^2

Find d, to minimize $Weight = \rho \times L \times w \times d$

where $Stress = \frac{6PL}{wd^2} \leq Stress_{allowed}$

Minimum Weight Design Algorithm

d chosen 1023 times



VIVA Results: d= 0.156” (0.155 exact)

Minimum weight = 1.09 lbs (1.082 exact)

Technology R&D - HUMAN & ROBOTIC TECHNOLOGY

"a bold new course into the cosmos"

Reconfigurable Scalable Computing (RSC)
for Space Apps - 4 yrs, $14.8M

\+ *SEE-Immune Reconfigurable FPGA*

with Sandia (DOE) & Xilinx

NASA Storaasli

ornl

RSC Team

Goddard Space Flight Center

THE UNIVERSITY OF QUEENSLAND
AUSTRALIA

Starbridge offers powerful
computation solutions for your world.

ASRC AEROSPACE
CORPORATION

Jefferson Lab
THOMAS JEFFERSON NATIONAL ACCELERATOR FACILITY

NATIONAL SECURITY AGENCY
UNITED STATES OF AMERICA

RSC Goals & Objectives

- Develop next-generation HPC leveraging:
  - FPGAs
  - Intellectual Property (IP)
    - Soft cores, processors
  - COTS software architectures
    - Multi-processor
    - Specialized
- Spinoff => next-gen avionics

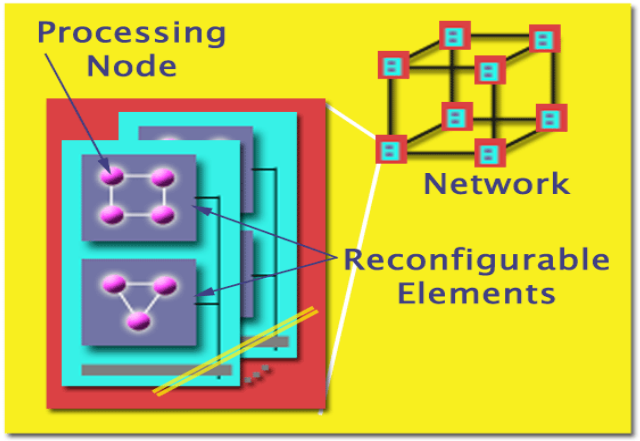
Scalable Stacked Modules

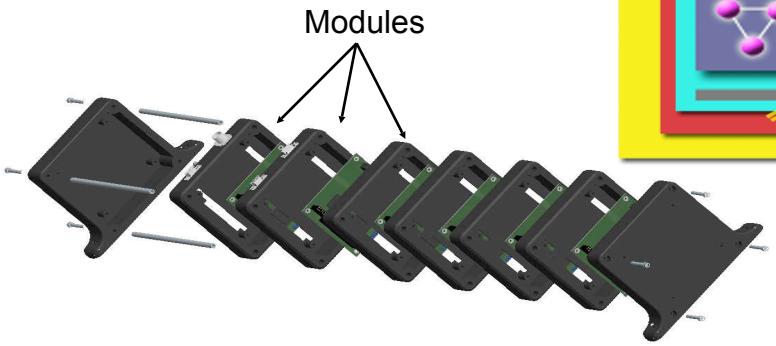
- Small, stackable
  - Mix-match modules for mission
- RSC modules:
  - Processing
  - IO
  - Network
  - Power
- RSC scales:

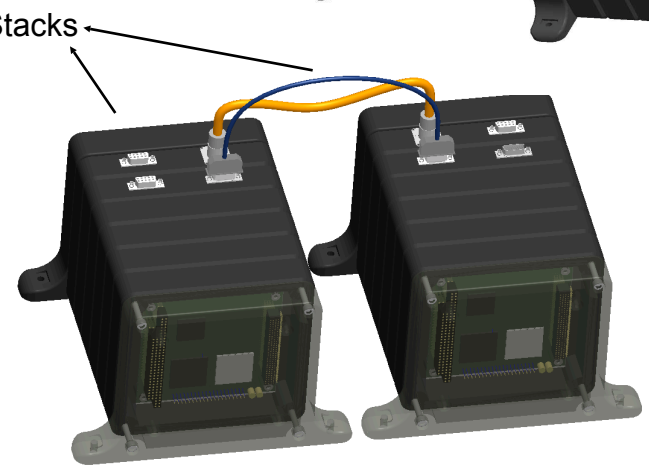
  # nodes/module

  # modules/stack

  # stacks in system







NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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+ NASA Home

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EXPLORATION SYSTEMS
Moon, Mars & Beyond...

Spirit & Opportunity Rovers

6 Radiation-tolerant FPGAs:

1M gates @ 100kRads

Next:

6M gates @ 200kRads

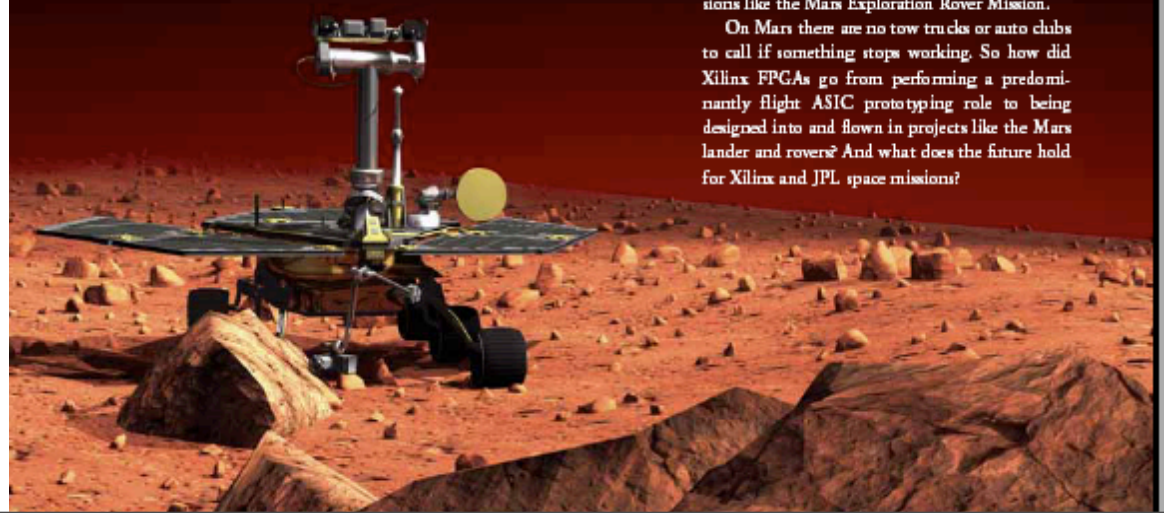
FPGAs on Mars

Xilinx FPGAs have transitioned from a flight ASIC prototyping platform to playing integral roles in the Mars Exploration Rover Mission.

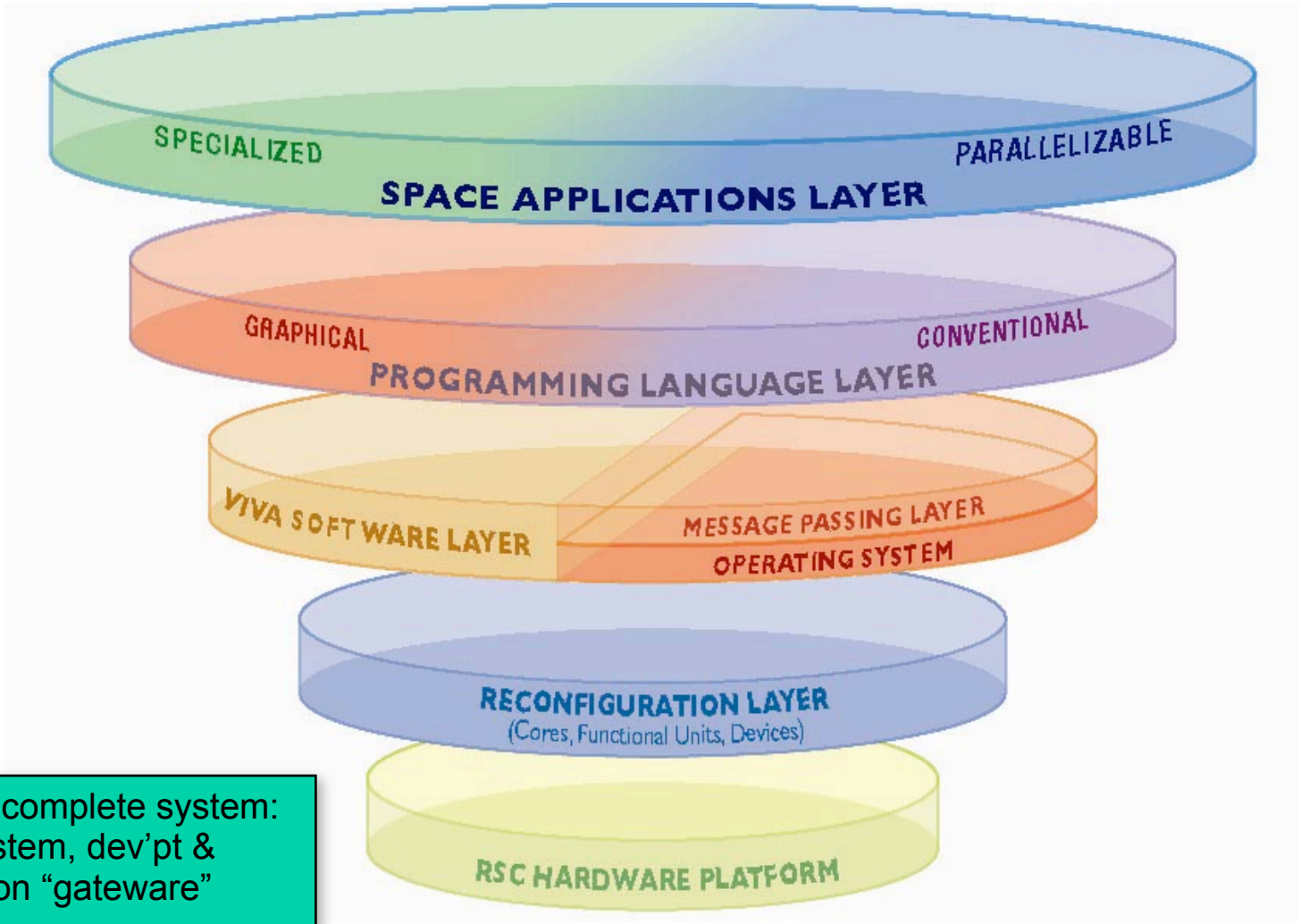
by David Ratter
Field Applications Engineer
Nu Horizons Electronics
dratter@nuhorizons.com

Selecting the correct components for any engineering project can be a critical and difficult choice. This is clearly true for engineers at the Jet Propulsion Laboratory (JPL) when they must select components used on high-stakes flight projects, and especially important on high-profile missions like the Mars Exploration Rover Mission.

On Mars there are no tow trucks or auto clubs to call if something stops working. So how did Xilinx FPGAs go from performing a predominantly flight ASIC prototyping role to being designed into and flown in projects like the Mars lander and rovers? And what does the future hold for Xilinx and JPL space missions?



Software Architecture



RSC to deliver complete system: hardware & system, dev'pt & demo/application "gateware"

Rover Demo

Tele-operated =>

Fuzzy-logic wireless control

4 Mecanum Wheels

RSC-controlled

3 Mecanum Wheels

Demo FPGA process power (imaging Apps)

Many Sensors:

- Stereo, IR & 360o Cameras
- Acoustic, proximity, ...

Rover Demo

Computational Speed-Up of Complex Durability Analysis of Large-Scale Composite Structures

Frank Abdi (Ph.D),
Ernie Cochran, Renly Dutton,
Alpha STAR Corporation Long Beach, CA USA

And

Olaf Storaasli (Ph.D)
Oak Ridge National Laboratory, Oak Ridge Tennessee, USA

AIAA Paper (April '08)

Alpha STAR Corporation (ASC)

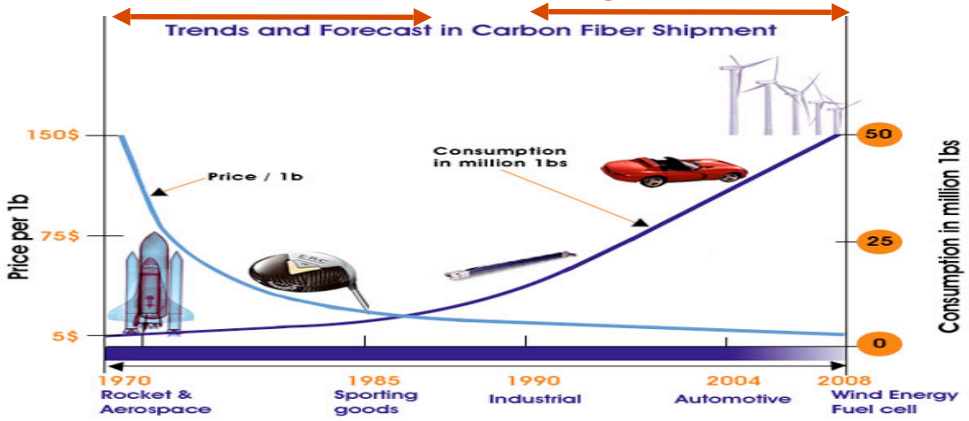
Background and Experience

- 19 years of successful industry experience in Advanced Composites and Metal materials and structures simulation, and FAA certification

- Forensic, and Failure Simulation of Large Scale industry Structures (e.g., US Space Shuttle Accident Investigation, Shuttle Return to Flight, Airbus 310, Boeing Delta Rocket tank, National Missile Defense (NMD) heat seeker, B1-B bird strike crash, helicopter blade anomalies, etc.

- Developed software (GENOA) design solutions for aerospace, automotive, & electronic chip industries in durability/reliability of composite materials and structures
- Industry verified computational tool integrated with MSC software

NASA NASTRAN Development (60's and 70's)



NASA GENOA Development (90's and Beyond)

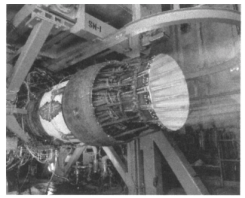
ASC CUSTOMERS

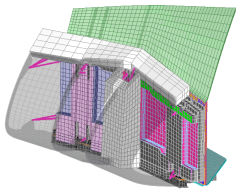
Industry Customers

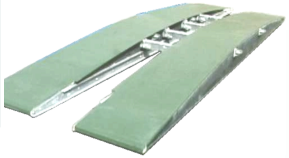
- Boeing
- Lockheed
- Northrop
- Stork Fokker
- Magna
- Delphi
- Alenia
- Sogeti High Tech
- EADS
- General Dynamics
- Bell Helicopter
- CTC Cable
- Goodrich
- Honda
- Honeywell
- Solar (Caterpillar)
- Siemens

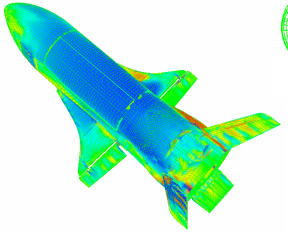
Government Agencies

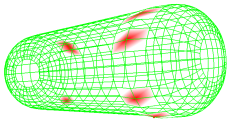
- US Army
- US Navy
- NASA
- SOCOM
- DOE (ORNL, PNL)
- SOCOM
- US Air Force
- JAXA

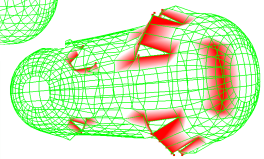










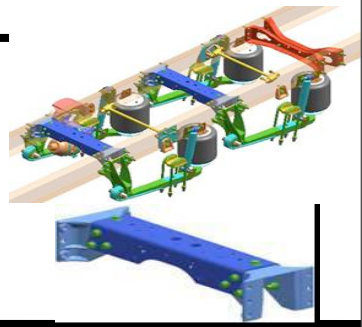
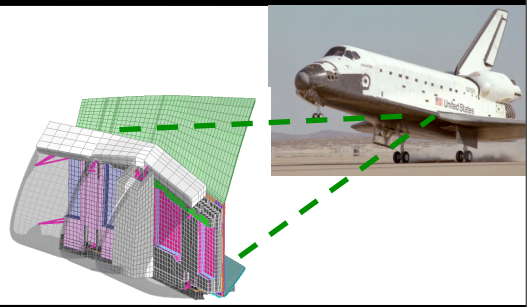
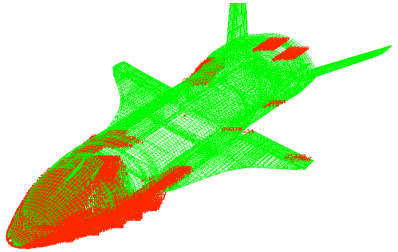


Objective

FEM Computing Time *Skyrockets for Larger Durability, Damage Tolerance, Optimization & Reliability Problems*

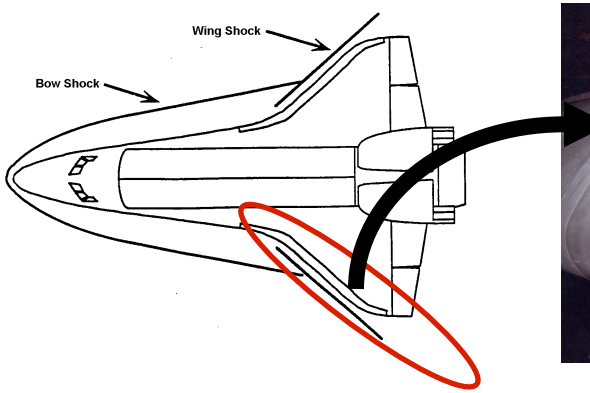
Problem	Problem Goal	Problem Size	Computing Time
Space Shuttle Foam Analysis	Predict Fracture Toughness, reliability	360 GB of data	> 2 Days
Composite Truck Chassis	Predict Residual Strength and Life	600,000 FEM	2 Weeks
Auto Composite Structure	Crash Analysis	400,00 FEM	8 Hours
HMWWV Structure	System Durability and Reliability Analysis	Ultra-large	Weeks on Multi-processors
Army Composite Bridge	Predicted Strength and Life After Battle Damage Repair	100,00 FEM	2 Days
Delphi/Delco Microelectronic Chip	Thermal Aging Analysis	>1,000,000 FEM	> 2 Weeks
Siemens combustor liner	Fatigue Life Prediction	Large	> 2 Weeks

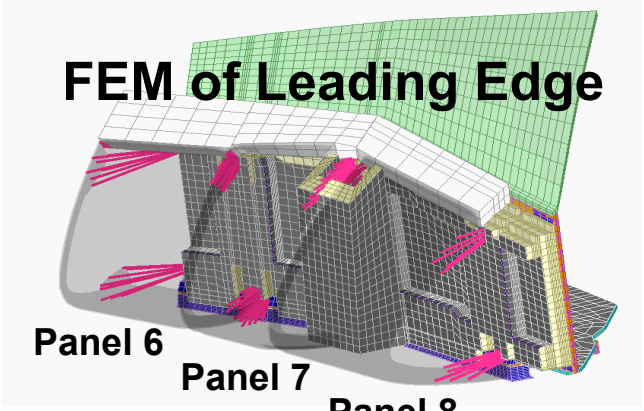
Aerospace Structures: Virtual Testing /Verification

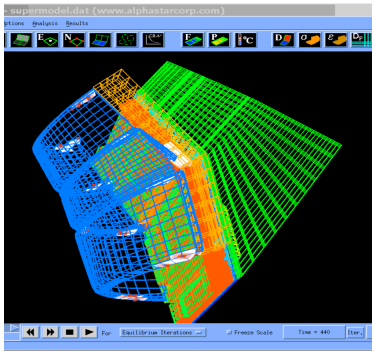
Organization	Project	Objective	
Delphi DOE ORNL	**Attachment Techniques for Heavy Truck Composite Chassis Members**	Rapid implementation of lightweight composite materials in Class 7/Class 8 vehicles via the development of advanced composite support lateral braces	
SOCOM	**HMWV Composite Weight Reduction**	Composite Replacement of Metal parts (strength, stiffness). Service load Evaluation	
NASA Columbia Accident Investigation Board	Shuttle Leading Edge Re-entry **Thermal-Structural**	Sequential damage scenario (~503 s) & wing Components structural failure	
Boeing-X37	Failure under **Launch Load** Environment (PSD)	Determine failure location, failure modes of composite Components	

Shuttle Accident Re-construction STS 107

Burn Through (Re-entry) Simulation



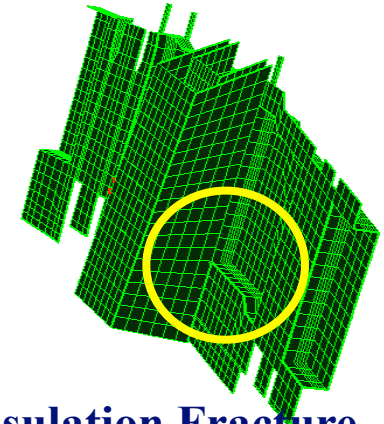




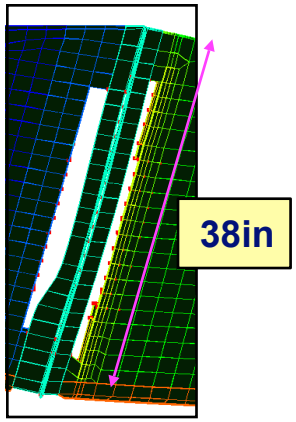
Fracture

(shown in RED)

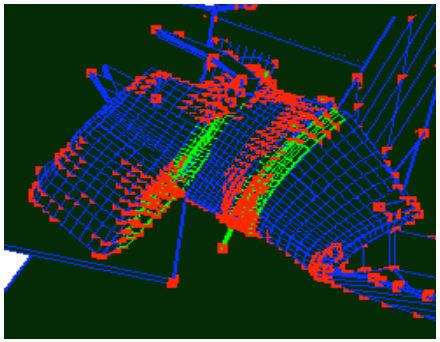
Time Line



Insulation Fracture
230 Sec



Spar Fracture
500 sec



RCC-Tseal Fracture
503 sec

Re-entry Simulation Recieved CAIB (Columbia Accident Investigation Board)/NASA Achievement Award 2004

Progressive Failure , Multi-Scale Modeling

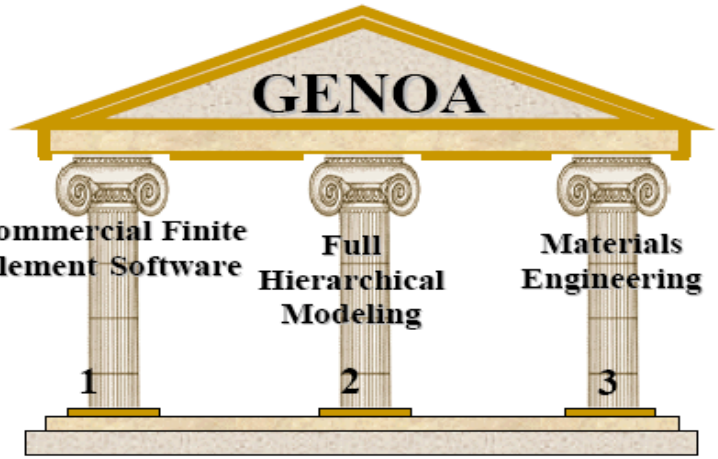


Figure 2-2. Three functional pillars of GENOA

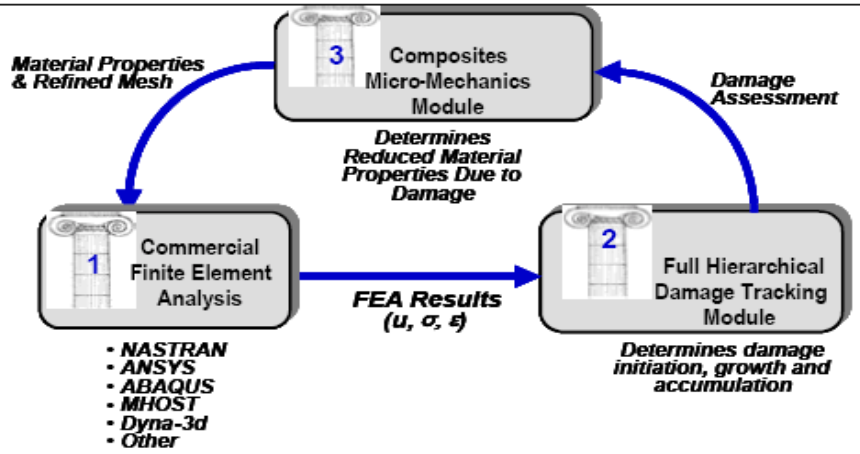
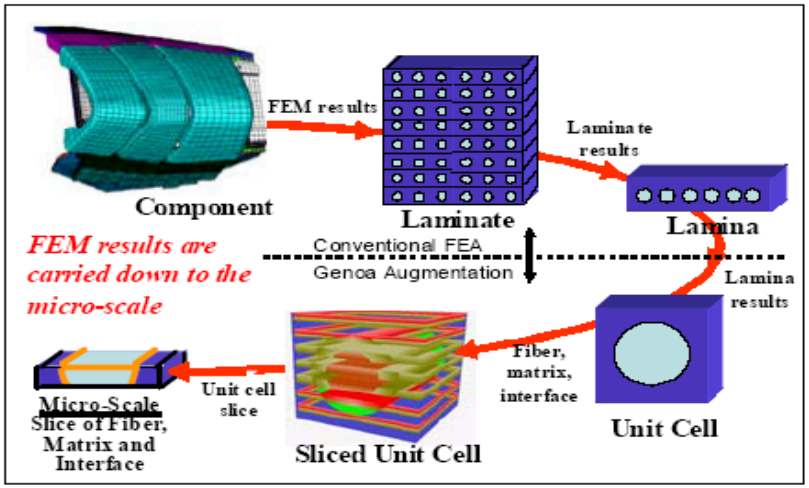
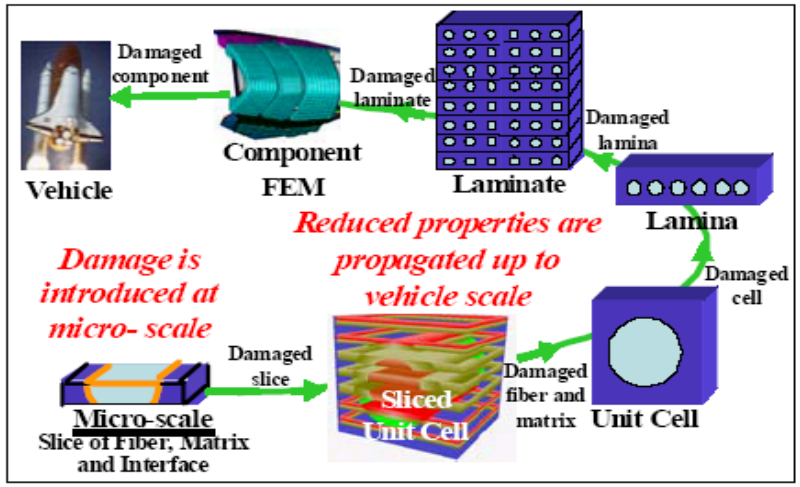


Figure 2-3. Flow chart illustrating the interactions between Genoa modules

Won NASA Software-of-the-Year Award



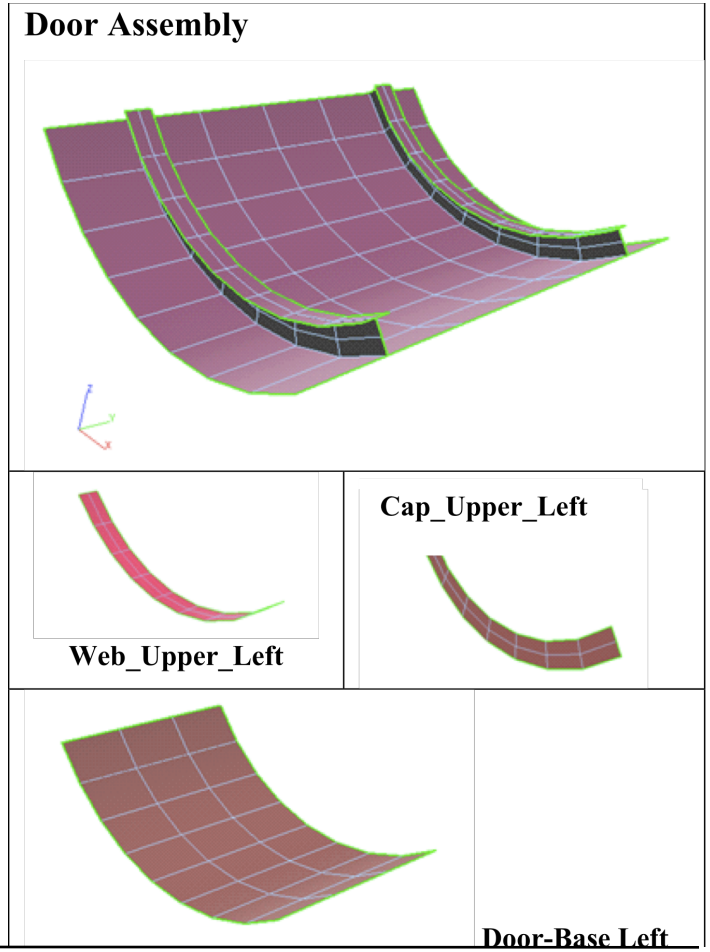
a) FEA results at the structural scale are propagated down to the microscale



b) . Reduced fiber and matrix properties at the microscale are propagated back up to the structural scale.

Solutions using Super Element, Forced Partitioning, Parallel Processing

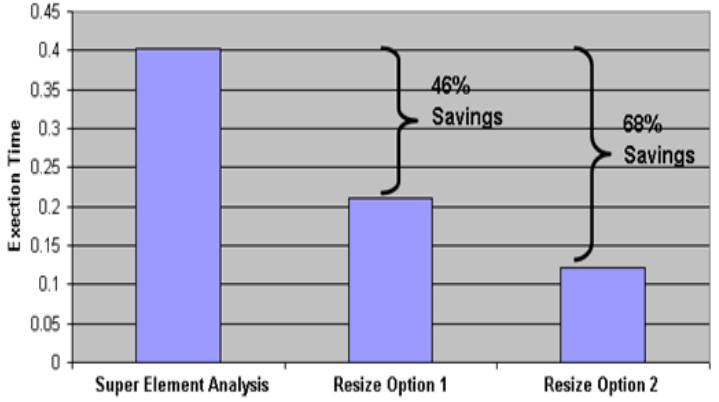
Door Assembly & Substructure Load Applied on Cap-Upper Left



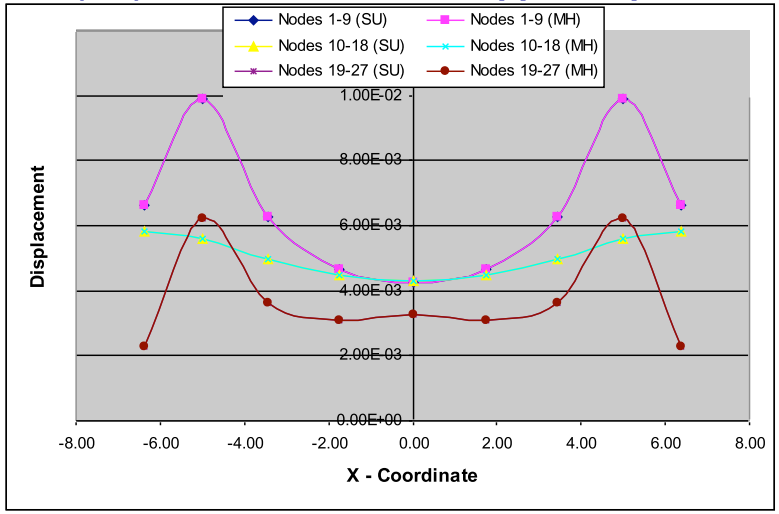
File for Generating Super Element

```
! DOEgrant_demo.cmd
! This is the MAESTRO command sequence
! to process the DOEgrant Demo.

*DEFINE_tree
  level 1
    Door_Base_left 1   Door_base_right 2
    Web_Upper_left 3   Web_Upper_right 4
    Cap_Upper_left 5   Cap_Upper_right 6
  level 2
    Cap_Web_left   7 5 3
    Cap_Web_right  8 6 4
  level 3
    Door_left      9 7 1
    Door_right     10 8 2
  level 4
    Door_Assy      11 7 10

*CREATE_data_base "demo"
  bulk_data "demo.dat"
  ripeel    "demo.rpl"

*CREATE_super_element_fem
  SE_name   "Door_Base_left"
  SE_name   "Web_Upper_left"
  SE_name   "Cap_Upper_left"

*STIFFNESS
  solver "mhost_v12 Door_Base_left"
  solver "mhost_v12 Web_Upper_left"
  solver "mhost_v12 Cap_Upper_left"
*END
```

Time Savings vs. Resize Option



Displacement Comparison of Super Element (SU) vs. Global FEM for Upper-Cap Left



FPGA (Field-Programmable Gate Array) Accelerator

FPGAs achieve remarkable computation time reductions (up to 100X faster than 2.2 GHz AMD Opteron)

Applications accelerated:

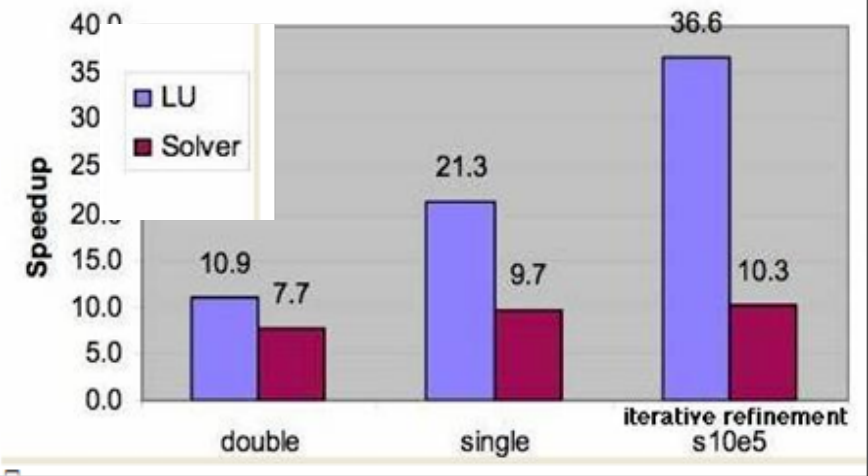
- human DNA genome sequence comparisons,
- molecular dynamics,
- weather/climate forecast/modeling,
- matrix multiplication & equation solution.

FPGA Accelerator Card ($299 to Academics)

Double precision(DP) matrix equation accuracy;

- challenges FPGAs (requires many arithmetic units),
- achieved via DP iterative refinement of SP parallel FPGA calculations.
- 36X speedup for matrix factor calculations (dominate large matrix equation solutions).

FPGA Speedup for Matrix factor/solve



Summary

Hardware: Exploits advanced FPGA systems

FPGAs: Rapid growth, inherently //, flexible, efficient

VIVA: Powerful & growing (tailor to NASA needs)

Applications: - Many Engineering algorithms (VIVA => FPGAs)

- GPS-VIVA => *CPU+FPGA accelerator*

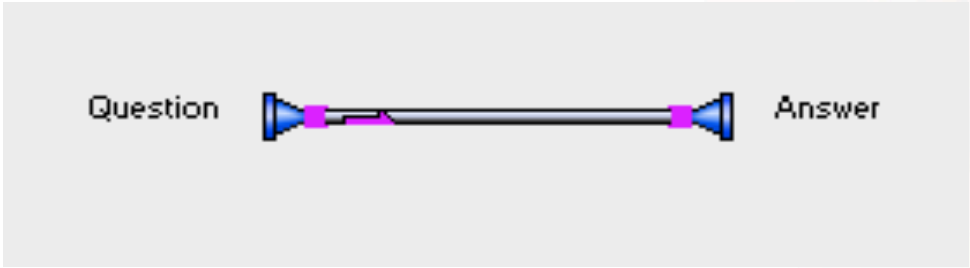
Speed: 640 ops/cycle (2×10^{11} ops/sec) measured

Future: Reconfigurable Scalable Computing for Space

Contact

Olaf O. Storaasli
Future Technologies Group
Google **Olaf ORNL**

THANK YOU



OAK RIDGE National Laboratory